AMENDED ABSTRACT

A phase detection system and method for use with a synchronous mirror delay ("SMD") or a delay-locked loop ("DLL") ~~in order to reduce~~ reduces the number of delay stages required~~,~~ and ~~therefore increase the~~ increases efficiency~~, is disclosed~~. The invention ~~includes taking~~ takes a clock input signal and ~~a~~ clock delay or feedback signal, each having timing characteristics, and ~~differentiating~~ differentiates between four conditions based upon ~~the~~ timing characteristics of the signals. The phase detector and associated circuitry ~~then~~ determines, based upon ~~the~~ timing characteristics of the signals, which ~~of a number of~~ phase conditions the signals are in. Selectors select the signals to be introduced into the ~~synchronous mirror delay or delay-locked loop~~ SMD or DLL by the timing characteristics of the phase conditions. The ~~system is able to utilize~~ invention utilizes the falling clock edge of the clock input signal~~,~~ and decreases the lock time ~~is decreased~~ under specific phase conditions. The invention increases ~~the~~ efficiency of the circuits by reducing the effective delay stages in the SMD or DLL while maintaining the operating range.

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